

**APPLICATION FOR UNITED STATES LETTERS PATENT**

by

**JOERN LUETZEN**

**ALBERT BIRNER**

**STEPHAN KUDELKA**

**HELMUT TEWS**

and

**ROLF WEIS**

for a

**METHOD AND STRUCTURES FOR INCREASING THE STRUCTURE DENSITY  
AND THE STORAGE CAPACITANCE IN A SEMICONDUCTOR WAFER**

SHAW PITTMAN LLP  
1650 Tysons Boulevard  
McLean, VA 22102-4859  
(703) 770-7900  
Attorney Docket No.: INF-115-US

# **METHOD AND STRUCTURES FOR INCREASING THE STRUCTURE DENSITY AND THE STORAGE CAPACITANCE IN A SEMICONDUCTOR WAFER**

## **BACKGROUND**

### **FIELD OF THE INVENTION**

[0001] The present invention relates generally to semiconductor fabrication and semiconductor structures.

### **BACKGROUND INFORMATION**

[0002] DRAM (dynamic random access memories) modules are a mass-produced product with many applications. On the one hand, smaller dimensions and, on the other hand, a higher number of memory cells for storing data, that is to say an increasing storage density, are demanded of new generations of DRAM modules. This results in the need to further reduce the cell size of an individual memory cell, comprising a storage capacitance and a selection transistor. Depending on the arrangement of the storage capacitance in or above a metalization plane, a distinction is made between memory cells of the "stacked capacitor" type and "trench capacitor" type. In the case of a memory cell of the "trench capacitor" type, a trench is formed in a monocrystalline semiconductor substrate of a semiconductor wafer below a metalization plane.

[0003] A dielectric, for example a nitride/oxide layer system, is provided along the trench wall. In the monocrystalline semiconductor substrate, a region which is doped by outdiffusion, for instance, and adjoins the trench forms a first electrode. In the trench, a counterelectrode is formed by deposition of highly doped polycrystalline silicon.

[0004] Reducing the cell size leads to trenches with a smaller electrode area and thus to storage capacitances having a lower electrical capacitance. In order to compensate for the loss of capacitance, it is necessary to increase the capacitance again in a different way by means of complicated new process technologies. Examples thereof are a higher doping of the electrodes in order to reduce the charge carrier depletion, the use of dielectrics with a high dielectric constant and the application of additional structures (HSG, hemispherical grains) on the trench wall in order to enlarge the surface.

[0005] A further possibility for increasing the capacitance consists in increasing the surface of the trench by means of a bottle-like extension in a lower section of the trench. The trench thus extends in the depth of the semiconductor substrate also partly into regions of the semiconductor substrate located below the selection transistors formed on the surface of the semiconductor substrate.

[0006] Figures 4A-C show plan view recordings taken by a scanning electron microscope, abbreviated to SEM hereinafter, of trenches of storage capacitances in different depths of a semiconductor substrate, said trenches being arranged in checkered fashion in alternation with unpatterned fields. The recordings each show an arrangement of structures which are based on a rectangular pattern in a mask layout and are transferred and etched into a semiconductor substrate in a conventional manner.

[0007] Figure 4A shows upper sections 8 of trenches of storage capacitances in the vicinity of the surface of the semiconductor substrate 6, said sections being provided with a protective layer that is resistant toward a bottle etching process.

[0008] A profile with a bottle-like extension 5 which is shown in Figure 4B is produced in each case in sections of the trenches formed below the protective layer. Between the sidewalls 7 of adjacent trenches, intermediate walls are formed from the material of the semiconductor substrate 6. The extent of the bottle-like extension 5 is limited by the demand for a minimum thickness of the intermediate walls. An excessively small thickness of the intermediate wall leads to a higher number of short circuits between the storage capacitances of adjacent memory cells on account of manufacturing tolerances.

[0009] Figure 4C represents the trenches in the region of a trench bottom 9 which terminates the trenches in the depth of the semiconductor substrate 6. They have a rectangular form with a smaller cross-sectional area than directly below the protective layer.

[0010] Overall, Figures 4A-C reveal, on the one hand, that although the electrode surface of the storage capacitance is enlarged by the bottle-like extension of the trench, on the other hand, the extent of the bottle-like extension is limited.

[0011] There is, accordingly, a need to provide improved fabrication techniques and structures for increasing storage capacitance.

#### **SUMMARY**

[0012] The present invention is based on the object of providing a method and a structure with which it is possible to further increase a structure density and/or a storage capacitance of an individual structure in a semiconductor substrate compared with conventional methods and structures.

[0013]           The invention provides for a method for increasing a structure size of main structures - formed in essential parts in a depth of a semiconductor substrate - by means of an etching process which expands the main structures in the depth of the semiconductor substrate, provision being made of the semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching, and the main structures being arranged in checkered fashion in a rectangular surface grid, at a surface of the semiconductor substrate, in each case in alternation with secondary structures formed in each case essentially in a section of the semiconductor substrate that is near the surface.

[0014]           The invention is explained below with reference to figures, identical reference symbols being used for mutually corresponding components.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0015]           Fig. 1 shows a diagrammatic illustration of an arrangement comprising mask and semiconductor wafer for carrying out the method according to the invention,

[0016]           Fig. 2 shows a diagrammatic illustration of an arrangement comprising mask and semiconductor wafer for carrying out a conventional method,

[0017]           Fig. 3 shows a diagrammatic longitudinal section through a trench etched into a semiconductor substrate,

[0018]           Figs. 4A-C show SEM plan view recordings of trenches in a semiconductor wafer in different depths,

[0019]           Figs. 5A-D show SEM plan view recordings of structures according to the invention in a semiconductor wafer in different depths,

[0020] Figs. 6A-F show SEM plan view recordings of structures according to the invention in a semiconductor wafer before and after a bottle etching in different depths,

[0021] Figs. 7A-B show diagrammatic plan views of surfaces of a semiconductor substrate processed conventionally and of a semiconductor substrate processed according to the invention, and

[0022] Fig. 8 shows an illustration of the functional dependence of the number of discharged memory cells AS on the time  $t_{Ret}$  in the case of semiconductor wafers processed according to the invention and in the case of semiconductor wafers processed conventionally.

#### **DETAILED DESCRIPTION**

[0023] A list of reference numerals used in the following description is provided below:

- 1 Semiconductor wafer
- 2 Marking
- 3 Mask
- 4 Trench
- 5 Extension
- 6 Semiconductor substrate
- 7 <110> sidewall
- 8 Upper part of the trench
- 9 Trench in the region of the trench bottom
- 10 Trench at the surface
- 11 <100> sidewall
- 12 Trench below the protective layer
- 131 Main structure
- 132 Secondary structure

- 14      Surface grid
- 151     Field for main structure
- 152     Field for secondary structure
- 161     Field for main structure below structure edge

[0024]            For the method according to the invention, a mask 3 and a semiconductor wafer 1 made of monocrystalline silicon are arranged in the manner shown in Figure 1. The semiconductor wafer 1 is provided with a marking 2 according to the invention, which marking is rotated by 45 degrees with respect to conventionally marked semiconductor wafers and identifies the  $\langle 100 \rangle$  crystal orientation of the silicon. By means of the marking, the mask is oriented to the crystal orientation in the semiconductor wafer. The mask structure is thus imaged along a different crystal orientation compared with conventional methods.

[0025]            For comparison purposes, an arrangement corresponding to the prior art is illustrated in Figure 2. Here the semiconductor wafer 1 is provided with a marking 2 pointing in the  $\langle 110 \rangle$  crystal orientation.

[0026]            Figure 3 shows a structure which is etched into a semiconductor substrate 6 and is designed as a trench 4. On account of a further etching step below a trench depth of about one micrometer, the trench has a bottle-like extension 5 for enlarging an electrode area of a storage capacitance to be processed from the trench. The upper section of the trench 8 is provided with a protective layer which prevents lateral etching into the semiconductor substrate 6 in regions near the surface.

[0027]            As previously explained, trenches of the type described can be seen in plan view in Figure 4. The trenches were imaged onto a nonrotated semiconductor wafer

using a checkered mask layout and subsequently etched into the semiconductor substrate 6.

[0028] Figure 4A illustrates the upper parts – provided with a protective layer – of the trenches 8, the sidewalls of which form an oval and the long side of which is arranged parallel to the  $\langle 110 \rangle$  crystal orientation. Such a side is called  $\langle 110 \rangle$  sidewall 7 for short hereinafter.

[0029] Deeper in the semiconductor substrate, approximately where the protective layer ends, the cross section illustrated in Figure 4B results, said cross section showing a bottle-like extension 5. Below the protective layer, the sidewalls form a rectangle with  $\langle 110 \rangle$  sidewalls 7. Intermediate walls formed from the semiconductor substrate 6 between the sidewalls of the individual trenches 8 have, at their thinnest points, a very small thickness of approximately 20 nanometers, which can lead to short circuits in the case of trenches processed to form storage capacitances, on account of manufacturing tolerances.

[0030] Figure 4C represents the trenches in the region of a trench bottom 9 terminating the trenches in the depth of the semiconductor substrate. There they have a rectangular form with a smaller cross-sectional area than directly below the protective layer. The sidewalls are again  $\langle 110 \rangle$  sidewalls 7.

[0031] The trenches shown in Figures 5A-D were produced by the method according to the invention. They are based on the same checkered mask layout of Figure 4. For this purpose, the mask layout is imaged onto a semiconductor wafer oriented according to the invention. Afterward, the trenches are etched into the semiconductor substrate 6 and each provided with a protective layer in upper sections. Figures 5A to



5D illustrate cross sections of the trenches in different depths parallel to the surface 10 of the semiconductor substrate 6.

[0032] In this case, Figure 5A shows a plan view of the trenches at the surface 10 of the semiconductor substrate 6. Figure 5B shows a cross section through the trenches in the region of the protective layer below the surface 10. The sidewalls of the upper sections of the trenches in each case form an oval whose long sides are oriented according to the invention parallel to the  $\langle 100 \rangle$  crystal orientation. Such a side is called  $\langle 100 \rangle$  sidewall 11 for short hereinafter. Figures 5C and 5D represent the cross sections of the trenches below the protective layer 12 in two different depths. The sidewalls of the trenches form a square with  $\langle 110 \rangle$  sidewalls 7 in cross section. The sidewalls of the upper section of a trench are thus rotated by 45 degrees with respect to the sidewalls of the lower section of the same trench. As can be seen when comparing Figure 4C with Figure 5D, the resulting rotated square cross section of the trenches in the region below the protective layer leads to an improved utilization of the area of the semiconductor substrate 6.

[0033] The improved utilization of area becomes clear from Figures 6A-F. The cross sections of the trenches produced according to the invention in figures 6A to 6C were recorded before the etching step (bottle etch) – leading to the bottle-like extension – in different depths and correspond to the cross sections of the trenches in Figures 5B to 5C.

[0034] The cross sections of the trenches after the etching step leading to the bottle-like extension can be seen on a larger scale in Figures 6D to 6F. The cross section – oval in plan view – in the upper section of the trenches with  $\langle 100 \rangle$  sidewalls 11 is

shown in Figure 6D. Figures 6E and 6F show the square cross sections with  $\langle 110 \rangle$  sidewalls 7 of the bottle-like extensions in two different depths, one above and one below the trench center. The perfect utilization of area in the depth of the semiconductor substrate can clearly be discerned here.

[0035]           The better utilization of a semiconductor substrate 6 by the method according to the invention is also illustrated with reference to Figures 7A-B.

[0036]           A pattern of main and secondary structures 131, 132 is formed on a surface of the semiconductor substrate 6, said pattern being oriented along a surface grid 14. The main and secondary structures 131, 132 are arranged alternately in checkered fashion in the surface grid 14.

[0037]           The surface grid 14 forms equally sized square fields 151, 152 in this example for illustration purposes. However, the method according to the invention also leads to an advantageous utilization of the semiconductor substrate 6 in the case of other divisions with unequally sized or expanded fields.

[0038]           The secondary structures 132 are essentially arranged in a section of the semiconductor substrate 6 near the surface between the surface of the semiconductor substrate 6 and a structure edge in the depth of the semiconductor substrate 6. By contrast, substantial parts of the main structures 131 are formed below the structure edge. The main structures 131 are conventionally expanded below the structure edge by means of a bottle etching process. After being expanded, the main structures 131 also extend, as illustrated in Figure 7A, into sections of the semiconductor substrate 6 which lie below the secondary structures 132.

[0039] In this case, the bottle etching process extends the main structures 131 in a manner independent of direction, so that the maximum possible extension of a main structure 131 is also restricted in the depth of the semiconductor substrate 6 to a field 151 assigned to the main structure 131. Sections of the semiconductor substrate which extend below the structure edge under fields 152 assigned to the secondary structures remain unused.

[0040] By contrast, those sections of the semiconductor substrate 6 below the substrate edge which are arranged below the fields 152 assigned to the secondary structures 132 are also made available, by the method according to the invention, for extension of the main structures 131.

[0041] For this purpose, as illustrated in Figure 7B, the surface grid 14 is oriented parallel to crystal faces of the semiconductor substrate 6 that are less resistant to etching. In the course of an area-selective etching process, the main structures 131 are formed in the depth of the semiconductor substrate 6 below the structure edge with sidewalls that are ideally rotated by 45 degrees with respect to the surface grid 14. If the rotated main structures 131 are subsequently expanded by means of a bottle etching below the structure edge, then an extended field 161 results for each main structure 131 as maximum extension.

[0042] The semiconductor substrate 6 below the structure edge can be completely assigned to the extended fields 161 and can thus advantageously be utilized almost completely for the extension of the main structures 131.

[0043] Figure 8 illustrates the functional dependence of the number of discharged memory cells AS on the time  $t_{Ret}$  - referred to as "retention time" - for DRAM

modules produced from semiconductor wafers processed in rotated fashion according to the invention and from semiconductor wafers processed in nonrotated fashion. Two DRAM modules in each case were examined for each curve. Curves A and B show the behavior of DRAM modules from semiconductor wafers processed in nonrotated fashion, curve B concerning memory cells having a storage capacitance reduced by 10% compared with the memory cells of curve A. Curves C and D show the behavior in the case of semiconductor wafers processed in rotated fashion according to the invention, curve D again concerning memory cells having a storage capacitance reduced by 10% compared with the memory cells of curve C. The significantly shallower profile of curves C and D compared with curves A and B describes a lengthened "retention time" in the case of semiconductor wafers processed in rotated fashion. The influence of the magnitude of the storage capacitance on the "retention time" also becomes clear from curves B and D. A reduced storage capacitance is accompanied by a decrease in the "retention time". In a time interval of  $128 \text{ ms} < t_{\text{Ret}} < 8 \text{ sec}$ , the following holds true: AS in the case of semiconductor wafers processed in rotated fashion is approximately  $0.5 \cdot$  AS in the case of semiconductor wafers processed in nonrotated fashion.

[0044]        Thus, according to the invention, before an etching process which expands the main structure in the depth, the longitudinal and transverse extents of main structures in the depth of the semiconductor substrate are oriented in rotated fashion with respect to the x, y axes of the surface grid. As a result, the sections of the semiconductor substrate which are located below secondary structures are made

available essentially completely for an extension of the main structures by means of the etching process which expands the main structure in the depth.

[0045] As a consequence, significantly larger dimensions and surfaces are possible for the main structures in the depth of the semiconductor substrate. If the main structures are formed in each case as electrical capacitances with electrode areas running along the surface, then it is possible to achieve higher capacitance values in comparison with conventional methods given the same space requirement on the surface of the semiconductor substrate by virtue of the better utilization of a volume of the semiconductor substrate. Given identical capacitance values, a large structure having the main and secondary structures can be embodied in a higher density by the method according to the invention.

[0046] The etching process which expands the main structure in the depth is referred to hereinafter, for simplification, as bottle etching process without this effecting a restriction to bottle etching processes in the narrower sense.

[0047] The term secondary structures also includes unpatterned sections of the surface of the semiconductor wafer.

[0048] One example of an alternate arrangement of main and secondary structures is a checkered arrangement (checkerboard). However, the method according to the invention does not necessarily presuppose the checkered arrangement of main and secondary structures.

[0049] The longitudinal and transverse extents of the main structures are oriented in a manner rotated by essentially 45 degrees with respect to the x, y axes of the surface grid. A maximum utilizability of the sections of the semiconductor substrate which

are arranged below the secondary structures results in this case. Intermediate walls between adjacent main structures are then formed in cross-sectional planes parallel to the surface of the semiconductor substrate with approximately the same thickness.

[0050]       The method according to the invention provides an area-selective etching process. To that end, provision is made of the semiconductor substrate comprising a crystalline material which has a crystal lattice with crystal faces that can be differentiated. In suitable etching processes, different etching resistances can be derived from the different properties of the crystal faces. The crystal lattice then has crystal faces that are less resistant to etching and crystal faces that are more resistant to etching.

[0051]       Preferably, a large structure having at least the main structures is now imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces that are less resistant to etching.

[0052]       Preferably, furthermore, the area-selective etching process is controlled in such a way that, in the depth of the semiconductor substrate below a structure edge determined by an extent of the secondary structures into the depth of the semiconductor substrate, primary sidewalls of the main structures that are constructed from the crystal faces that are less resistant to etching are substituted by secondary sidewalls constructed from the crystal faces that are more resistant to etching. The orientation of the crystal faces that are more resistant to etching is rotated in customary semiconductor substrates with respect to the orientation of the crystal faces that are less resistant to etching, so that in this way the orientation - which is intended

according to the invention and is rotated with respect to the surface grid - of the longitudinal and transverse extents of the main structure in the depth of the semiconductor substrate is achieved in a particularly advantageous manner.

[0053]           The large structures are imaged onto the semiconductor substrate by means of a mask having an essentially rectangularly patterned mask layout.

[0054]           The semiconductor substrate is preferably provided as a semiconductor wafer to be processed in semiconductor process technology. In the processing of the semiconductor wafer, a further advantage of the method according to the invention is exhibited in the fact that only one marking which identifies a crystal orientation in the semiconductor wafer and defines the position of the semiconductor wafer with respect to the mask has to be modified, to be precise in such a way that it is rotated by 45 degrees with respect to the conventional marking and, according to the invention, identifies the orientation of the crystal faces that are less resistant to etching. The processing of the semiconductor wafers, that is to say the process steps of lithography, dry etching and implantation, is then effected unchanged with respect to nonrotated semiconductor wafers corresponding to the prior art.

[0055]           According to the invention, provision is to be made of the main structures at the surface of the semiconductor substrate in essentially oval fashion.

[0056]           Monocrystalline silicon is preferably chosen as the material of the semiconductor substrate. For an area-selective etching process in the course of which  $\langle 100 \rangle$  crystal faces are etched more rapidly than  $\langle 110 \rangle$  crystal faces, the surface grid is oriented in accordance with a  $\langle 100 \rangle$  crystal orientation of the monocrystalline silicon.

[0057] Preferably, in the course of a further processing of the semiconductor substrate, the main structures are functionally designed as storage capacitances and the secondary structures are essentially designed as selection transistors assigned to the storage capacitances.

[0058] The method according to the invention is explained in more detail below using the example of a storage capacitance for a DRAM memory cell:

[0059] A mask which prescribes the arrangement at least of main structures is provided with a rectangular pattern for patterning deep trenches each serving as a storage capacitance. The structures on the mask are imaged onto a semiconductor wafer provided with a marking according to the invention, which marking points in the  $\langle 100 \rangle$  crystal orientation, by means of an exposure device. In this case, the longitudinal side of the imaged rectangles is oriented parallel to the  $\langle 100 \rangle$  crystal orientation in the semiconductor wafer. The trenches are subsequently etched by means of a dry etching step whose etching speed is dependent on the crystal orientation, in the semiconductor wafer crystal faces with a  $\langle 100 \rangle$  orientation being etched more rapidly than crystal faces with a  $\langle 110 \rangle$  orientation. Only crystal faces with a  $\langle 110 \rangle$  orientation then remain after a specific etching time. By means of a further etching step, the deep trenches etched in the dry etching step are extended in bottle-like fashion below a trench depth of about one micrometer. Above one micrometer, the trenches are provided with an etching-resistant protective layer which prevents lateral etching into regions of the semiconductor substrate which are near the surface.



[0060] Before the bottle etching which leads to a bottle-like extension of the trench, the main structure which is produced in the course of the above-described method according to the invention in a semiconductor wafer is an etched trench which has, in an upper section adjoining the surface of the semiconductor wafer, a profile which is oval in plan view, with longitudinal sides parallel to the  $\langle 100 \rangle$  crystal orientation, that is to say  $\langle 100 \rangle$  sidewalls. In a lower section below the protective layer, that is to say for instance below one micrometer, the trench has a square profile with  $\langle 110 \rangle$  sidewalls. In this case, the length of the square diagonals essentially corresponds to the longitudinal extent of the oval profile in the upper part of the structure. The upper oval part of the structure is thus rotated by 45 degrees with respect to the lower square part since the two crystal orientations  $\langle 100 \rangle$  and  $\langle 110 \rangle$  are at an angle of 45 degrees with respect to one another.

[0061] In the case of a mask layout as used for the production of DRAM modules, the rectangles to be imaged are arranged in checkered fashion. The thickness of an intermediate wall between the sidewalls of the individual trenches is significantly increased compared with the semiconductor wafer processed in nonrotated fashion.

[0062] Hereinafter, checkered arrangement is understood to be a pattern in which the rectangles to be imaged on the mask are arranged in rows and are at the same constant distance from one another in each row. The rows are in each case arranged offset with respect to one another in such a way that, in the row lying below or above one row, two rectangles of said one row again have a rectangle situated between them essentially centrally. The distances between the rectangles are chosen such that the rectangles do not touch one another. By virtue of the square cross section and the

rotated form of the lower part of the trenches, the volume in the semiconductor wafer is utilized significantly better compared with the conventionally processed semiconductor wafer.

[0063]           After a further etching step having a duration of about 90 seconds, which brings about a bottle-like extension in the lower section of the trench, the trench in the depth of the semiconductor substrate has a profile that is square in plan view. The thickness of the intermediate walls comprising the semiconductor substrate between the individual trenches is of the order of magnitude of 100 nanometers, instead of about 20 nanometers in the case of semiconductor wafers processed in nonrotated fashion. It is thus possible to etch significantly larger extensions of the trenches, thereby increasing the electrical capacitance of storage capacitances formed from the trenches. Moreover, the square cross section of the lower part of the trenches leads to an optimum filling of the area of the semiconductor wafer in the depth of the semiconductor substrate.

[0064]           In order to reduce leakage currents in a DRAM cell, comprising a selection transistor and a storage capacitance, the semiconductor wafer from which the DRAM cell is produced is processed according to the method according to the invention.

[0065]           A similar method for reducing leakage currents is also described in WO 00/02249.

[0066]           The required size of a storage capacitance depends, inter alia, on the leakage currents that occur. A typical value for a DRAM cell storage capacitance comprising a deep trench is the 40 fF/cell, in which the total cell leakage current is of the order of magnitude of 10 to 15 fA/cell. The latter contains various components, such as, for

example, leakage currents through the dielectric, leakage currents along an interface between the semiconductor substrate and a structure that insulates the storage capacitance in the region near the surface (STI, shallow trench isolation), or leakage currents in the region of the interfaces of source and drain of the selection transistor.

[0067] In accordance with the method according to the invention for reducing leakage currents in a DRAM cell having a selection transistor and a storage capacitance, the leakage current along the interface between the semiconductor substrate and the STI structure is now significantly reduced. The reduction of the leakage current can be attributed to a lower density of defect locations (trap) along the interfaces oriented according to the invention, since the size of the leakage current is correlated with the number of defect locations and the number of defect locations is reduced in the case of a changed crystal orientation.

[0068] A reduction of the total cell leakage current directly decreases the required capacitance. An advantage afforded by a lower capacitance is that the trench depth of the trench serving as capacitance can be reduced. As a result, the etching time could be reduced by the same order of magnitude as the trench depth, thereby significantly increasing the throughput of this process step.

[0069] Statistics based on examinations of a plurality of DRAM modules reveal that the total cell leakage currents of a DRAM cell in the case of the semiconductor wafer processed in a manner rotated by 45 degrees according to the invention are reduced by more than 30% compared with the semiconductor wafer processed in nonrotated fashion.

[0070]           The reduction of the cell leakage current leads to an equivalent increase in the time interval after which the charge in one of the DRAM cells has decreased on account of leakage currents to an extent such that the charge stored in a memory cell has to be refreshed. This time interval is referred to as "retention time".

[0071]           A DRAM cell containing a storage capacitance having a structure according to the invention in a semiconductor wafer which has been processed in accordance with the method according to the invention has an increased storage capacitance, reduced leakage currents and thus an increased "retention time".

[0072]           The foregoing disclosure of the preferred embodiments of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many variations and modifications of the embodiments described herein will be apparent to one of ordinary skill in the art in light of the above disclosure. The scope of the invention is to be defined only by the claims appended hereto, and by their equivalents.

[0073]           Further, in describing representative embodiments of the present invention, the specification may have presented the method and/or process of the present invention as a particular sequence of steps. However, to the extent that the method or process does not rely on the particular order of steps set forth herein, the method or process should not be limited to the particular sequence of steps described. As one of ordinary skill in the art would appreciate, other sequences of steps may be possible. Therefore, the particular order of the steps set forth in the specification should not be construed as limitations on the claims. In addition, the claims directed to the method

and/or process of the present invention should not be limited to the performance of their steps in the order written, and one skilled in the art can readily appreciate that the sequences may be varied and still remain within the spirit and scope of the present invention.